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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,882	02/27/2004	Paul A. Farrar	303.673US3	9145

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,882	FARRAR, PAUL A.	
	Examiner	Art Unit	
	Dao H Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-79* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0204 & 0804*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 02/27/2004 through 08/03/2004, claims 1-79 are active in this application.

Acknowledges

2. Receipt is acknowledged of the following items from the Applicant.

a. Information Disclosure Statement (IDS) filed on 02/27/2004 and 08/03/2004. The references cited on the PTOL 1449 form have been considered.

Applicant is requested to cite any relevant prior art if being aware on form PTO-1449 in accordance with the guidelines set for in M.P.E.P. 609.

b. This application is a Divisional of the co-pending Application Serial No. 10/117,041 filed 04/05/2002, which is a Divisional of Application No. 09/484,002 filed 01/18/2000, now patent No. 6,376,370.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is

requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. The claim is objected to for the following reason:

Claim 8 recites the limitation "the polyimide layer" on line 5;

Claim 14 recites the limitation "transistors" on line 4;

There are insufficient antecedent basis for these limitations in the claims.

In claim 18, line 5, there is a repeat or duplication of the phrase "each conductive structure".

Appropriate corrections are required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claim(s) 50, 51-55 and 57-58 is/are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,350,678 to Pramanick et al.

Regarding claim 50, Pramanick discloses an integrated circuit, as shown in figs. 2-3, comprising:

a first level via 112 in a first insulator layer 110 connecting to a transistor in a substrate (see col. 1, lines 16-23, col. 5, lines 13-20);

a first conductive structure formed over the first level via 112 in the first insulator layer 110, the first conductive structure including:

a first barrier/adhesion layer 120 disposed on the first level via 112;

a first seed layer 122 disposed on the first barrier/adhesion layer 120; and

a first metal line 202 disposed above the first seed layer 122;

a second insulator layer 108 containing the first conductive structure;

a second conductive structure having a portion disposed on the first metal line 202 of the first conductive structure, the second conductive structure including:

a second barrier/adhesion layer 124 disposed on the first metal line 202;

a second seed layer 126 disposed on the second barrier/adhesion layer 124; and

a second metal line 204 disposed above the second seed layer 126.

Regarding claims 51-55 and 57-58, Pramanick discloses the integrated circuit comprising all claimed limitations. See col. 5, lines 34-41; col. 6, line 66 to col. 7, line 22.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 1-49, 56, 59-79 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,350,678 to Pramanick et al., in view of the following remarks.

Regarding claims 1-4 and 8-10, Pramanick discloses an integrated circuit, as shown in figs. 2-3, comprising:

a substrate including one or more devices (col. 1, lines 13-22; col. 5, lines 13-22);

a first insulating (or insulator) layer 110 overlying the substrate having one or more first level vias 112 connecting to the one or more devices in the substrate; and

a second insulating layer 108 overlying the first insulating (insulator) layer 110, the second insulating layer 108 including one or more conductive structures formed

above and connecting to the one or more first level vias 112, each of the one or more conductive structures including:

a first level metal line 202;

a barrier/adhesion layer 120 formed on the number of first level vias 112; and

a seed layer 122 formed at least between a portion of the barrier/adhesion layer 120 and the first level metal line 102.

Pramanick is silent about the thicknesses of the barrier/adhesion layer, the seed layer, and the first insulating layer; or about the second insulating layer being a polymer layer, a foamed polymer layer, or a polyimide layer, or the first insulating layer includes a Si_3N_4.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the barrier/adhesion layer and the seed layer of Pramanick can be designed and/or modified to have any suitable thickness since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges (or working thickness(es)) involves only routine skill in the art. In re Aller, 105 USPQ 233.

In addition, it is well known that the second insulating layer can be of any suitable material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. (See also U.S. Patent No. 5,824,599 to Schacham-Diamand et al.; column 5, line 59 to column 6, line 4).

Regarding claims 5-7, 11-13, Pramanick discloses the device comprising all claimed limitations. See col. 5, lines 13-41.

Regarding claim 14, Pramanick discloses an integrated circuit, as shown in figure2-3, comprising:

a substrate including one or more devices (col. 1, lines 16-23; col. 5, lines 13-28);

an insulator layer 110 overlying the substrate having one or more first level vias 112 connecting to the one or more devices in the substrate; and

an oxide layer 101/108/116 overlying the insulator layer 110 including one or more conductive structures formed above and connecting to the one or more first level vias, each of the one or more conductive structures including:

a layer of titanium or zirconium 120 disposed on a first level via of the number of first level vias 112;

a first layer of aluminum 202 on the layer of titanium or zirconium 120; a layer of copper 126 on the first layer of aluminum 202; and

a second layer of aluminum 204 on the layer of copper 126.

Pramanick is silent about the thicknesses of the layer of titanium, layers of aluminum and layer of copper.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that these layers can be designed and/or modified to have any suitable thickness since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges (or working thickness(es)) involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 15-17, Pramanick discloses the circuit comprising all claimed limitations. See also the rejection of claim 1.

Regarding claims 18-22, Pramanick discloses an integrated circuit, as shown in figs. 2-3, comprising:

a number of first level vias 112 in a first insulator layer 110 connecting to a number of silicon devices in a substrate, and

a first number of conductive structures formed over and connecting to the number of first level vias 112 in the first insulator layer 110, each conductive structure of the first number of conductive structures including:

a barrier layer disposed on a first level via of the number of first level vias 112;

a seed layer of copper 122 on the layer of zirconium; and

a copper metal line 202 formed on the seed layer of copper 122; and

a second insulator layer surrounding the first number of conductive structures.

Pramanick is silent about the thickness of the barrier layer and the seed layers, as well as the material of the barrier layer and the second insulator layer.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the barrier layer and the seed layer of Pramanick can be designed and/or modified to have any suitable thickness since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges (or working thickness(es)) involves only routine skill in the art. In re Aller, 105 USPQ 233.

In addition, it is well known that the barrier layer and the second insulator layer can be of any suitable material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. (See also U.S.

Patent No. 5,824,599 to Schacham-Diamand et al.; column 5, line 59 to column 6, line 4).

Regarding claim 23, Pramanick discloses an integrated circuit, as shown in figs. 2-3, comprising:

a number of first level vias 112 in a first insulator layer 110 connecting to a number

of silicon devices in a substrate;

a first number of conductive structures formed over and connecting to the number of first level vias 112 in the first insulator layer 110, each conductive structure, comprising:

a first barrier/adhesion layer 120 disposed on a first level via of the number of first level vias;

a first seed layer 122 formed on at least a portion of the barrier/adhesion layer; and

a first core conductor 200 formed on the first seed layer 122;

a second insulating layer 108 surrounding the first number of conductive structures; and

a second number of conductive structures include a number of second level vias 106 and a number of second level metal lines, wherein the second number of conductive structures are formed over and connect to the first number of conductive structures, and wherein each of the second number of conductive structures

includes:

a second barrier/adhesion layer 124;

a second seed layer 126 formed on at least a portion of the barrier/adhesion 124 layer; and

a second core conductor 204 formed on the second seed layer 126.

Pramanick is silent about the thicknesses of the barrier/adhesion layers and the seed layers.

However, it would have been obvious to one having ordinary skill in the art at the time the invention was made that the barrier/adhesion layers and the seed layers of Pramanick can be designed and/or modified to have any suitable thickness since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges (or working thickness(es)) involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claims 24-29, Pramanick discloses the integrated circuit comprising all claimed limitations. See the above remarks and also the rejections of claims 1-4.

Regarding claims 30-43 and 56, Pramanick discloses integrated circuits comprising all claimed limitations. See more detail from the rejections of claims 1-7.

Regarding claims 66-79, Pramanick discloses a system, as shown in figs. 2-3, comprising all claimed limitations (see further details in the rejection of claim 1-7), except for the system further comprising a processor coupled to the integrated circuit.

However, since the system of Pramanick is a metallization system used to connect individual devices together to perform desired circuit functions, it is common and well known in the art that such device could and should include a processor to perform the required tasks.

9. Claim(s) 44-49 and 59-65 is/are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,350,678 to Pramanick et al., in view of Jung et al., U.S. Patent No. 6,376,368.

Regarding claim 44, Pramanick discloses an integrated circuit, as shown in figs. 2-3, comprising:

a first level via 112 in a first insulator layer 110 connecting to a transistor in a substrate (see col. 1, lines 16-22; and col. 5, lines 13-29);

a conductive structure formed over the first level via 112 in the first insulator layer 110, the conductive structure including:

a barrier/adhesion layer 120 disposed on the first level via 112;

a seed layer 122 on the barrier/adhesion layer 120; and

a metal line 202 disposed above the seed layer 122, and

a second insulator layer 108 containing the conductive structure.

Pramanick does not discloses a titanium silicide liner that contains the first level via;

However, Jung discloses a contact structure, as shown in figs. 10-15, comprising titanium silicide liner 61a'/73a' that contains the via hole VH. See col. 9, line 7 to col. 10, line 44.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Pramanick to include a titanium silicide liner as that of Jung in order to prevent an occurrence of a junction spiking phenomenon. See col. 1, lines 20-27 of Pramanick.

Regarding claims 45-49, Pramanick/Jung disclose the integrated circuit comprising all claimed limitations. See also the rejections of claims 1-7.

Regarding claim 59, Pramanick discloses an integrated circuit, as shown in figs. 2-3, comprising:

a first level via 112 in a first insulator layer 110 connecting to a silicon device in a substrate (see col. 1, lines 16-23, col. 5, lines 13-20);

a first conductive structure formed over the first level via 112 in the first

insulator layer 110, the first conductive structure including:

a first barrier/adhesion layer 120 disposed on the first level via 112;

a first seed layer 122 disposed on the first barrier/adhesion layer 120; and

a first metal line 202 disposed above the first seed layer 122;

a second insulator layer 108 containing the first conductive structure;

a second conductive structure having a portion disposed on the first metal line 202 of the first conductive structure, the second conductive structure including:

a second barrier/adhesion layer 124 disposed on the first metal line 202;

a second seed layer 126 disposed on the second barrier/adhesion layer 124; and

a second metal line 204 disposed above the second seed layer 126.

Pramanick does not disclose a titanium silicide liner containing the first level via;

However, Jung discloses a contact structure, as shown in figs. 10-15, comprising titanium silicide liner 61a'/73a' that contains the via hole VH. See col. 9, line 7 to col. 10, line 44.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Pramanick to include a titanium silicide liner as that of Jung in order to prevent an occurrence of a junction spiking phenomenon. See col. 1, lines 20-27 of Pramanick.

Regarding claims 60-65, Pramanick/Jung disclose the integrated circuit comprising all claimed limitations. See the rejection of claims 1-7.

Conclusion

10. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao H. Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday, 9:00 AM – 6:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571)272-1787. The fax numbers for all communication(s) is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
August 30, 2004